# January 2022
## M. Sc. III Semester Examination

**PHYSICS**
Third Paper : Digital Electronics

Time 3 Hours]

[Max. Marks : Regular 85 / Private 100
[Min. Marks : Regular 28 / Private 33

**Note : This question paper is meant for all Regular and Private students. Answer all five questions. All questions carry equal marks. The blind candidates will be given 60 minutes extra time.**

1. Perform the following operation using 2's complement subtraction method. Explain 2's complement in brief :
(a) 1101010 – 1010101
(b) 10010 – 10001
(c) 01010 – 10110
(d) 11110 – 11101.

OR

Perform the following conversions :
(a) $(161.23)_{10} = (?)_2$
(b) $(152.34)_8 = (?)_{10}$
(c) $(101011010.110)_2 = (?)_{10}$
(d) $(AB23)_{16} = (?)_{10} = (?)_2$.

2. (a) Reduce the given equation using Karnaugh Map :

$$F(A, B, C, D) = \Sigma(0, 2, 4, 6, 7, 8, 10, 12, 13, 14) + d(5, 15)$$

where $d$ = don't care term.

(b) Perform the following conversion :
(i) $(526) = (?)_{BCD}$
(ii) $(1010110)_2 = (?)_{GRAY}$.

OR

(a) Explain full adder using suitable diagram.
(b) What do you understand by Universal Gates ? Explain.

3. (a) Implement 4 × 1 multiplexer using 2 × 1 multiplexer.
(b) Explain race ground condition. Also explain how it can be avoided.

OR

(a) Implement J-K flip flopping using R-S flip flop.
(b) Design and explain 3 bit shift register.

4. (a) Design asynchronous decade counter and explain.
(b) Explain 4 bit ring counter. How it is different from 4 bit binary counter ?

OR

(a) Explain 4 bit Up-Down counter using suitable diagram.
(b) Explain the difference between synchronous and asynchronous counter.

5. (a) Describe the necessity of ADC and DAC.
(b) Explain successive approximation analog to digital conversion using suitable diagram.

OR

(a) What is the largest value of output voltage from an 8-bit DAC that produce 1.0 V for a digital input of 00110010.
(b) Explain R-2K ladder network digital to analog converter.

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